## REMARKS

Please reconsider the application in view of the following remarks. Applicant thanks the Examiner for carefully considering this application.

**Disposition of Claims**

Claims 16-26 are currently pending in this application. Claims 16 and 26 are independent. The remaining claims depend, directly or indirectly, from claim 16.

**Rejections under 35 U.S.C. § 102**

Claims 16, 25, and 26 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,369,855 ("Chauvel"). This rejection is respectfully traversed.

The claimed invention relates to a receiver/decoder with memory including a buffer section and a FIFO section. Depending on the needs of the application module and/or the nature of the message, the claimed invention enables a message to be read out to a port without awaiting complete writing of the message, or be read out to an application either before the complete message is written or after the complete message is written.

Thus, the claimed invention is a decoder with improved message handling. The message is either handled by the FIFO or the buffer, depending on the nature of the message and/or the requirements of the application module. Further, the message of the claimed invention is a finite message, with a starting point and an ending point of the message.

For anticipation under 35 U.S.C. § 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present.

The Applicant respectfully asserts that Chauvel does not teach or suggest a receiver/decoder comprising a memory including a buffer section and a FIFO section, where a message is written and read from one port of the receiver/decoder to another port, either after completion of the writing of the message, or without waiting for completion of the writing of the message.

Chauvel relates to an improved audio-visual circuit for receiving a transport stream with audio/video decoders for decoding audio and video portions of a transport stream. Chauvel discloses that the circuit receives a transport stream from the output of a forward error correction (FEC) device. Subsequently, all packets requiring further processing or containing relevant information are sent to the internal RAM. (*See* Chauvel, col. 10, ll. 9-10 and 16-19). The RAM operates like a first-in first-out (FIFO) buffer and stores two types of transport packets: data that is routed to SDRAM without further processing and data that needs further processing by the ARM. (*See* Chauvel, col. 10, ll. 29-34). At this stage, the payload data processed by the ARM, both audio and video data is stored in external SDRAM. *The video and audio decoders then read the bitstream from SDRAM and process it accordingly.* (*See* Chauvel, col. 10, ll. 62-64).

Turning to the rejection of the claims, the Examiner asserts that Chauvel discloses each and every limitation of independent claim 16. The Applicant respectfully disagrees. As described above, Chauvel discloses that video/audio decoders read the digital bitstream from SDRAM themselves, and thus, Chauvel cannot possibly disclose or suggest *a control signal* sent from the video/audio decoders to the buffer controller because the video/audio decoders are themselves reading the digital bitstream. For the same reason, Chauvel does not need to contemplate a control signal in response to which the buffer reads data out to the application.

Further, independent claim 16 of the present invention clearly states that it is possible to start outputting the message before completion of the writing of the message. Thus, the message of the claimed invention has a finite starting point and ending point. However, in a digital bitstream, there is no finite end to the stream. The only "end" of a bitstream is the end of the transmission of the bit stream, in which case it clearly does not make sense to output the digital bitstream before the completion of the transmission of the bit stream, as required by independent claim 16. For this reason, the digital bit stream of Chauvel is distinct from the message of the claimed invention, and Chauvel fails to disclose or suggest outputting a message before completion of the writing of the message. Further, Chauvel very clearly describes the architecture for his system, which is implemented in one chip, and as such the architecture is very difficult to modify. Thus, Chauvel does not consider the option of reading a message before writing it completely to memory and/or reading the message after it is completely written in memory.

In view of the above, it is clear that Chauvel fails to disclose or suggest each and every limitation of independent claim 16. Thus, claim 16 is patentable over Chauvel. Dependent claim 25 is patentable for at least the same reason. Further, Independent claim 26 includes similar allowable subject matter and is patentable over Chauvel for at least the same reasons as claim 16. Accordingly, withdrawal of this rejection is respectfully requested.

**Rejections under 35 U.S.C. § 103**

Claims 17-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel. This rejection is respectfully traversed.

With respect to the rejection of the claims, the Examiner admits that Chauvel fails to explicitly disclose the FIFO controller includes an occupancy detector for detecting the state of

occupancy of the FIFO section, detecting overflow and underflow of the FIFO section, and thresholds relating to the FIFO section. *See* Office Action mailed May 12, 2005, page 4. However, the Examiner takes Official Notice that it is well known in the art to detect buffer occupancy, buffer overflow and underflow, including thresholds thereto, for the purpose of preventing loss of incoming data when buffer overflow has occurred to is impending. Applicant respectfully disagrees with the Examiner's assertion and requests that the Examiner provide evidence to support this position either in the form of prior art or by providing a declaration of personal knowledge pursuant to 37 C.F.R. 1.104 (d) (2).

Further, even if including an occupancy detector is well know in the art, as described above, Chauvel fails to disclose a control signal in response to which the buffer reads data out to the application, as recited in independent claim 16. Further, Chauvel fails to disclose or suggest a receiver/decoder that enables a message to be read as soon as a part of it is written in memory, while at the same time enabling the possibility to completely write a message in a buffer before handing it to the requesting application module. In fact, Chauvel does not provide this option, and does not even contemplate the need for this option.

Thus, in view of the above, claim 16 is patentable over Chauvel. Claims 17-20 are patentable over Chauvel for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 21-23 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel in view of Campanella and further in view of Powell. This rejection is respectfully traversed.

As described above, Chauvel fails to disclose or suggest each and every element of independent claim 16. Further, neither Campanella nor Powell supplies that which Chauvel lacks.

In particular, Campanella relates to a satellite direct radio broadcast receiver for extracting a broadcast channel and service control header from time division multiplexed transmissions. Specifically, Campanella discloses a method for receiving one of a plurality of prime rate channels transmitted via downlink signals from a satellite. (*See* Campanella, Abstract). Powell relates to an integrated circuit memory that includes processing capability on the same chip, on one or both of an address path and data path between a set of access registers and a memory array so that an address can be generated, checked or manipulated and/or data can be manipulated or compared with a reference pattern of data. (*See* Powell, Abstract).

However, neither Campanella nor Powell disclose or suggest a control signal sent to a buffer, in response to which the buffer reads out data to an application module. Further, Campanella and Powell fail to disclose or suggest providing the option of reading a message from a FIFO before the complete message is written, or reading the message after the complete message is written to memory.

Further, Applicant notes that there is no motivation to combine the teachings of Campanella and Powell. The Examiner cannot combine prior art references to render a claimed invention obvious by merely showing that all the limitations of the claimed invention can be found in the prior art references. Instead, there must a suggestion or motivation to combine the references within the prior art references themselves. In other words, regardless of whether prior art references can be combined, there must an indication within the prior art references *expressing desirability* to combine the references. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990) (emphasis added). Further, the present application *cannot be used a guide* in reconstructing elements of prior art references to

render the claimed invention obvious. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (emphasis added).

In the present case, there is no expression of desirability in either Campanella or Powell that would cause one skilled in the art to turn to the teachings of the other. In fact, neither Campanella nor Powell relate to improved message handling using a buffer section and a FIFO section of memory. Rather, Powell discloses generating, checking, and manipulating *memory addresses*, not message handling. Campanella discloses providing service providers with direct access to a satellite and choices as to the amount of space segment that is purchased and used. In addition, Campanella relates to providing a low-cost radio receiver unit capable of receiving time division multiplexed downlink bit stream. (*See* Campanella, col. 1, ll. 65-67 and col. 2, ll. 1-2). Further, Campanella has nothing to do with generating, checking, or manipulating memory addresses or processing on a single chip. Thus, it is clear that no motivation to combine these two references exists.

In view of the above, it is clear that claim 16 is patentable over Chauvel, Campanella, and Powell, whether considered separately or in combination. Dependent claims 21-23 are patentable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Claim 24 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel, Campanella, and Powell, and further in view of U.S. Patent No. ("O'Toole"). This rejection is respectfully traversed.

As an initial matter, Applicant notes that various combinations of one or more of four references have been used in rejecting the claims of the present application. The purported reconstruction of the claimed invention by reliance on such a large number of references including, for example, a method for receiving one of a plurality of prime rate channels transmitted via

downlink signals from a satellite (U.S. Patent No. 5870390) is not appropriate. It is abundantly clear that the Examiner, using the present application as a guide, has selected isolated features of the various relied-upon references to arrive at the limitations of the claimed invention. Use of the present application as a "road map" for selecting and combining prior art disclosures is wholly improper. *See* MPEP § 2143; *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132 (Fed. Cir. 1985) (stating that "[t]he invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time"); *In re Fritch*, 972 F.2d 1260 (Fed. Cir. 1992) (stating that "it is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious . . . . This court has previously stated that 'one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.'"); *In re Wesslau*, 353 F.2d 238 (C.C.P.A. 1965) (stating that "it is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art").

As described above, none of Chauvel, Campanella, and Powell disclose the limitations of independent claim 16. Further, O'Toole fails to supply that which the aforementioned references lack. Specifically, O'Toole relates to storing of multiple data frames in a single buffer, which provides efficient utilization of memory space as large size buffers are used to hold more than a single data frame. O'Toole discloses a *single buffer*, and not two types of memory sections for improved message handling, as required by independent claim 16. Further, O'Toole fails to

disclose or suggest providing the option of reading a message from a FIFO before the complete message is written, or reading the message after the complete message is written to memory.

In view of the above, it is clear that claim 16 is patentable over Chauvel, Campanella, Powell, and O'Toole, whether considered separately or in combination. Dependent claim 24 is patentable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

**Conclusion**

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 11345/017001).

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Respectfully submitted,

By _____
for Jonathan P. Osha T. Chyau Liang
Registration No.: 33,986 #48,885

OSHA · LIANG LLP
1221 McKinney St., Suite 2800
Houston, Texas 77010
(713) 228-8600
(713) 228-8778 (Fax)
Attorney for Applicant